Claim Amendments

Please amend claims 18-22, 26, 28, 30, and 32-35 as follows:

Please cancel claims 1-17, 23 and 31 as follows:

Please add new claims 38-44 as follows:

Claims as Amended

1-17 (cancelled)

18. (currently amended) A contact interconnect structure comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first ~~set of dielectric layers comprising a first~~ contact layer overlying the active contact regions comprising a first plurality of metal filled openings extending through the first contact layer thickness to ~~provide electrical communication to~~ the active contact regions;

a second ~~set of dielectric layers comprising a second~~ contact layer overlying the first contact layer comprising a second plurality of metal filled openings, each of said second plurality of metal filled openings extending through the ~~first~~ second contact layer thickness ~~to provide electrical communication~~ to a respective one or more of the first ~~contact region~~ plurality of metal filled openings;

wherein, each of the first ~~and~~ second plurality of metal filled openings ~~comprise a bottom portion having a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5~~ form a continuous contact interconnect structure having an aspect ratio of less than about 4.5 with respect to a

respective contact layer.

19. (currently amended) The contact interconnect structure of claim 18, wherein the bottom portion of said contact interconnect structure has a maximum width of less than about ~~50~~ 70 nanometers and an aspect ratio of less than about 4.5.

20. (currently amended) The contact interconnect structure of claim 18, further comprising an overlying metallization layer in electrical communication with the ~~contact layer~~ second plurality of metal filled openings.

21. (currently amended) The contact interconnect structure of claim 18, wherein the first and second ~~set of dielectric~~ contact layers comprise[[s]] PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, silicon oxynitride, or combinations thereof.

22. (currently amended) The contact interconnect structure of claim 18, wherein the first and second ~~set of dielectric~~ contact layers comprise lowermost portions selected from the group consisting of silicon carbide, nitrogen doped silicon oxide, silicon nitride, and silicon oxynitride.

23. (cancelled)

24. (original) The contact interconnect structure of claim 18, wherein the first and second first and second plurality of metal filled openings comprise conductive materials selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta.

25. (original) The contact interconnect structure of claim 18, wherein the active contact regions are selected from the group consisting of source and drain regions and gate electrodes.

26. (currently amended) The contact interconnect structure of claim [[18]] 25, wherein the gate electrode comprises a gate structure having a gate length of less than about 45 nm.

27. (original) The contact interconnect structure of claim 18, wherein the active contact regions comprise a conductive material selected from the group consisting of Ti, Co, Ni, Pt, W, $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, TiN, and TaN.

28. (currently amended) The contact interconnect structure of claim 18, wherein the first and second ~~set of dielectric~~ contact

layers comprises an uppermost portion selected from the group consisting of a hardmask layer and a BARC layer.

29. (original) The contact interconnect structure of claim 18, wherein the first and second plurality of metal filled openings comprise a shape selected from the group consisting of circular and rectangular.

30. (currently amended) The contact interconnect structure of claim 18, wherein the first and second ~~first and second first and second~~ plurality of metal filled openings are selected from the group consisting of vias, contact holes, butt contact interconnects, local interconnects, and interconnect lines.

31. (cancelled)

32. (currently amended) A contact interconnect structure comprising:

at least [[a]] first and second stacked contact layers comprising a respective first and second plurality of metal filled openings extending through the first and second contact layers ~~thickness~~ to a contact region comprising an active

transistor region ~~provide electrical communication to overlying and underlying conductive regions~~ to form a stacked contact interconnect structure;

wherein, each of the at least first and second plurality of metal filled openings comprise a bottom portion having a maximum width of less than about 70 nanometers and an aspect ratio of less than about 3.3 with respect to a respective contact layer.

33. (currently amended) The contact interconnect structure of claim 32, wherein the bottom portion has a maximum width of less than about 50 nanometers and an aspect ratio of less than about 4.5.

34. (currently amended) The contact interconnect structure of claim 32, wherein the ~~at least a~~ first and second contact layers comprise[[s]] ~~one of an overlying~~ an underlying ~~second contact layer~~ etch stop layer.

35. (currently amended) The contact interconnect structure of claim 32, wherein the ~~underlying conductive~~ active transistor region[[s]] ~~comprise active conductive regions~~ is selected from the group consisting of source and drain regions and gate

electrodes.

36. (original) The contact interconnect structure of claim 35, wherein the gate electrode comprises a gate structure having a gate length of less than about 45 nm.

37. (original) The contact interconnect structure of claim 32, wherein the overlying conductive regions comprise a metallization layer.

38. (new) A stacked contact interconnect structure for achieving a high aspect ratio comprising:

a semiconductor substrate comprising CMOS devices including active contact regions;

a first contact layer overlying the active contact regions comprising a first metal filled opening extending through the first contact layer thickness to the active contact regions;

a second contact layer overlying the first contact layer comprising a second metal filled opening extending through the second contact layer thickness to the first metal filled openings;

wherein, each of the first second metal filled openings have about the same width to form a stacked contact interconnect structure having an aspect ratio of less than about 4.5 with respect to a respective contact layer.

39. (new) The contact interconnect structure of claim 38, wherein the bottom portion of said contact interconnect structure has a maximum width of less than about 70 nanometers and an aspect ratio of less than about 4.5.

40. (new) The contact interconnect structure of claim 38, wherein the first and second contact layers comprise PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, nitrogen doped silicon oxide, fluorine doped silicon oxide, SiC, silicon nitride, silicon oxynitride, or combinations thereof.

41. (new) The contact interconnect structure of claim 38, wherein the first and second contact layers comprise lowermost etch stop layer selected from the group consisting of silicon carbide, nitrogen doped silicon oxide, silicon nitride, and silicon oxynitride.

42. (new) The contact interconnect structure of claim 38, wherein

the first and second first and second plurality of metal filled openings comprise conductive materials selected from the group consisting of Cu, W, Al, AlCu, TiN, TiW, Ti, TaN, and Ta.

43. (new) The contact interconnect structure of claim 38, wherein the active contact regions are selected from the group consisting of source and drain regions and gate electrodes.

44. (new) The contact interconnect structure of claim 38, wherein the active contact regions comprise a conductive material selected from the group consisting of Ti, Co, Ni, Pt, W, $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, TiN, and TaN.